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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/693,491	10/27/2003	Shunpei Yamazaki	12732-097002	3131

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EXAMINER	
RICHARDS, N DREW	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/693,491	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	N. Drew Richards	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,25 and 26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,25 and 26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 10/105,282.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/27/03,7/16/04*, 2/1/05, 4/15/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 3, 5, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa et al. (JPPAT 2001-035808, Suzawa) in view of Hibino et al. (JP 2001-010685, Hibino).

With regard to claim 1, Suzawa discloses in figure 12 a semiconductor device. Suzawa discloses in figures 6 and 12 a semiconductor layer (601 in figure 6) over an insulating surface (102 in figure 12). Suzawa discloses in figures 6 and 12 a gate insulating film (602 in figure 6) on said semiconductor layer. Suzawa discloses in figures 6 and 12 a gate electrode (118 – 123 in figure 12 and 603b and 604b in figure 6) on said gate insulating film. Suzawa discloses in figures 6 and 12 wherein said semiconductor layer comprises a channel formation region (206, 210, 214, 218, 222, or 228 in figure 12), at least one LDD region (207, 211, 215, 219, 223, or 229 in figure 12) in contact with said channel formation region, and a source region (208, 213, 216, 221, or 225 in figure 12) or a drain region (209, 212, 217, or 220 in figure 12) in contact with said LDD region. Suzawa discloses in figures 6 and 12 wherein said gate electrode has a taper shape. Suzawa discloses in figures 6 and 12 wherein said gate electrode comprises a laminate of a fourth electrode (603b in figure 6) and a fifth electrode (604b

in figure 6). Suzawa does not teach wherein said gate electrode comprises a laminate of a fourth electrode, a fifth electrode and a sixth electrode. Hibino teaches in figure 3b a gate electrode (12) having a taper shape wherein the gate electrode comprises a laminate of a fourth electrode (13), a fifth electrode (14) and a sixth electrode (15). It would have been obvious to one of ordinary skill in the art at the time of the present invention to form the three layered gate electrode of Hibino in the device of Suzawa in order to provide a low resistance aluminum gate electrode and to prevent erosion of the gate electrode during formation of the device as stated by the English language translation of Hibino (USPAT 6529251) in column 3, lines 14 – 18 (a more specific application of why this is true can be found in column 6, lines 27 – 29 and 39 – 43, as well as column 7, lines 38 – 45).

With regard to claim 3, Suzawa teaches in paragraphs [0011] that fourth and fifth electrode layers at the top and bottom of a gate stack can comprise W or Ti. Hibino discloses in paragraphs 68 – 69 wherein top and bottom electrode layers in a gate stack comprise Ti, and a middle gate stack layer comprises Al. Therefore, it would have been further obvious in the method of Suzawa and Hibino wherein the fourth conductive film is a conductive film comprising W or a material including W as its main component, the fifth conductive film is a conductive film comprising Al or a material including Al as its main component and the sixth conductive film is a conductive film comprising Ti or a material including Ti as its main Component.

With regard to claim 5, Suzawa discloses in figure 12 said fourth electrode is overlapped with said LDD region through said gate insulating film.

With regard to claim 25, Suzawa discloses in figure 18a wherein said semiconductor device is selected from the group consisting of a computer.

3. Claims 2, 4, 6, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzawa in view of Yudasaka et al. (USPAT 5953582, Yudasaka) and Hibino et al. (JP 2001-010685, Hibino).

With regard to claim 2, Suzawa discloses in figure 12 a semiconductor device. Suzawa discloses in figures 6 and 12 a semiconductor layer (601 in figure 6) over an insulating surface (102 in figure 12). Suzawa discloses in figures 6 and 12 a gate insulating film (602 in figure 6) on said semiconductor layer. Suzawa discloses in figures 6 and 12 a gate electrode (118 – 123 in figure 12 and 603b and 604b in figure 6) on said gate insulating film. Suzawa discloses in figures 6 and 12 wherein said semiconductor layer comprises a channel formation region (206, 210, 214, 218, 222, or 228 in figure 12), at least one LDD region (207, 211, 215, 219, 223, or 229 in figure 12) in contact with said channel formation region, and a source region (208, 213, 216, 221, or 225 in figure 12) or a drain region (209, 212, 217, or 220 in figure 12) in contact with said LDD region. Suzawa is silent to the impurity concentrations of the LDD, source and drain regions. Yudasaka teaches in figure 26 and column 26, lines 8 – 15 wherein an LDD region (642b) comprises a impurity region for giving one conductivity at a concentration of 1×10^{17} to 1×10^{20} cm^{-3}, and one of said source region (642a) and said drain region (643a) comprises said impurity element at a concentration of 1×10^{20} to 1×10^{21} cm^{-3} (the disclosed ranges of 3×10^{18} to 1×10^{19} cm^{-3} and 1×10^{20} cm^{-3} make the

claimed range obvious, see MPEP 2144.05 I). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the impurity concentrations of Yudasaka in the method of Suzawa in order to use an impurity concentration that is well known in the art for LDD and source/drain regions, respectively. Suzawa discloses in figures 6 and 12 wherein said gate electrode has a taper shape. Suzawa discloses in figures 6 and 12 wherein said gate electrode comprises a laminate of a fourth electrode (603b in figure 6) and a fifth electrode (604b in figure 6). Suzawa and Yudasaka do not teach wherein said gate electrode comprises a laminate of a fourth electrode, a fifth electrode and a sixth electrode. Hibino teaches in figure 3b a gate electrode (12) having a taper shape wherein the gate electrode comprises a laminate of a fourth electrode (13), a fifth electrode (14) and a sixth electrode (15). It would have been obvious to one of ordinary skill in the art at the time of the present invention to form the three layered gate electrode of Hibino in the device of Suzawa and Yudasaka in order to prevent erosion of the gate electrode during formation of the device as stated by the English language translation of Hibino (USPAT 6529251) in column 3, lines 14 – 18 (a more specific application of why this is true can be found in column 6, lines 27 – 29 and 39 – 43, as well as column 7, lines 38 – 45).

With regard to claim 4, Suzawa teaches in paragraphs [0011] that fourth and fifth electrode layers at the top and bottom of a gate stack can comprise W or Ti. Hibino discloses in paragraphs 68 – 69 wherein top and bottom electrode layers in a gate stack comprise Ti, and a middle gate stack layer comprises Al. Therefore, it would have been further obvious in the method of Suzawa and Hibino wherein the fourth conductive film

is a conductive film comprising W or a material including W as its main component, the fifth conductive film is a conductive film comprising A1 or a material including A1 as its main component and the sixth conductive film is a conductive film comprising Ti or a material including Ti as its main Component.

With regard to claim 6, Suzawa discloses in figure 12 said fourth electrode is overlapped with said LDD region through said gate insulating film.

With regard to claim 26, Suzawa discloses in figure 18a wherein said semiconductor device is selected from the group consisting of a computer.

Double Patenting

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1 – 6, 25 and 26 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1, 3, and 7 of U.S. Patent No. 6,657,260 in view of Yudasaka. Claims 1, 3, and 7 teach all of the claim limitations of Yudasaka, but fail to specifically teach a channel formation region, an LDD region, source/drain regions, and that the gate electrode has a tapered structure. Yudasaka provides teaching for these features and the reasons for combination are obvious to one of ordinary skill similar to the 103 rejections above.

Response to Arguments

6. Applicant's arguments filed 2/1/05 have been fully considered but they are not persuasive.

Applicant argues that since Suzawa teach a structure in which a gate electrode is formed over a semiconductor layer and Hibino teach a structure in which a gate electrode is formed below the semiconductor layer, nothing in Hibino would have motivated one of ordinary skill in the art to employ Hibino's gate electrode in Suzawa's device. This is not persuasive. Hibino teach a structure that allows a highly conductive aluminum gate to be formed without incurring defects caused by erosion of the gate electrode. Thus, it would have been obvious to use an aluminum gate to take

advantage of aluminum's high conductivity, and obvious to use the three layer gate electrode to prevent erosion of the aluminum gate. This motivation is applicable to a structure where the gate is formed above or below the semiconductor layer as in both cases it is advantageous to employ a highly conductive gate and in both cases defects from erosion would advantageously be avoided.

Applicant further argues that Suzawa does not use an aluminum film and thus does not face the erosion problem such that one of ordinary skill in the art would not have been motivated to use the electrode structure of Hibino. Suzawa discusses the use of aluminum in TFT wiring and states that it is conventionally used because of its ease of workability, it electrical resistivity, and its chemical resistance. Suzawa then states problems associated with aluminum wiring such as diffusion of aluminum atoms into a channel forming regions. See Suzawa paragraph 0004. Hibino provides an electrode structure that allows aluminum to be used as a gate electrode (TFT wiring) which provides a TiN layer between the aluminum layer and the channel such that the aluminum atoms don't diffuse into the channel formation regions. Hibino gives specific motivation for using their three layer electrode including aluminum. Thus, in reading the references as a whole, one is clearly motivated to use an aluminum gate and to use the three layer electrode structure of Hibino to provide the aluminum gate without defects caused by erosion. Thus, one of ordinary skill in the art at the time of the invention would be motivated to combine the references to render the claims obvious.

Applicant last argues that the double-patenting rejection is improper since "it is not proper to turn to the disclosure of Yudusaka '260 for purposes of making a double-

patenting rejection." This argument is not persuasive. First, U.S. Patent No. 6,657,260 and Yudasaka are different references. Yudasaka is U.S. Patent No. 5,953,582. Second, the double-patenting rejection is an obviousness-type with a secondary reference. Yudasaka is the secondary reference relied upon to render obvious the features of the instant claims that were not recited in the claims of U.S. Patent No. 6,657,260. The application of Yudasaka as a secondary reference in the double-patenting rejection is proper and thus the rejection is considered proper.

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to N. Drew Richards whose telephone number is (571) 272-1736. The examiner can normally be reached on Monday-Friday 9:00-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NDR

TOM THOMAS
SUPERVISORY PATENT EXAMINER